LAB EXAMINATION

NAME: SOUMYADIP GHOSH

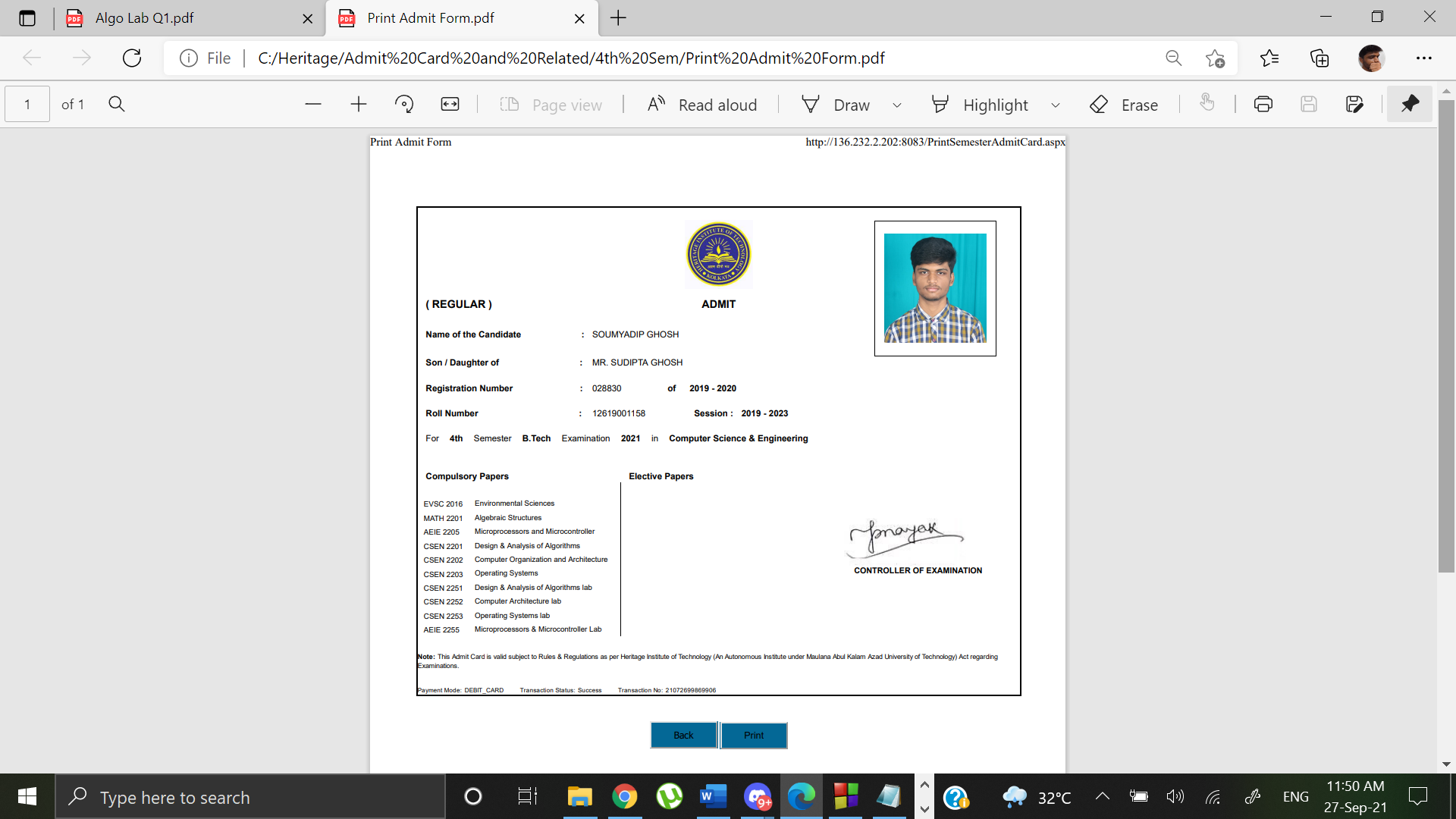
STREAM: CSE-A

ROLL NUMBER: 1951007

AUTONOMY ROLL NUMBER: 12619001158

SUBJECT: COMPUTER ARCHITECTURE LAB

SUBJECT CODE: CSEN 2252



**SET 5**

**Question:**

Design and simulate dataflow model for AND, NOT using NOR Gate

**AND USING NOR**

**Dataflow Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity and\_using\_nor is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : out STD\_LOGIC);

end and\_using\_nor;

architecture Behavioral of and\_using\_nor is

begin

C<= (A NOR A) NOR (B NOR B);

end Behavioral;

**Test Bench Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity and\_using\_nor\_tb is

-- Port ( );

end and\_using\_nor\_tb;

architecture Behavioral of and\_using\_nor\_tb is

component and\_using\_nor is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : out STD\_LOGIC);

end component;

signal A1 : STD\_LOGIC := '0';

signal B1 : STD\_LOGIC := '0';

signal C1 : STD\_LOGIC;

begin

uut: and\_using\_nor port map (A=>A1, B=>B1, C=>C1);

stim\_proc: process

begin

wait for 100ns;

A1<= '0';

B1<= '0';

wait for 100ns;

A1<= '0';

B1<= '1';

wait for 100ns;

A1<= '1';

B1<= '0';

wait for 100ns;

A1<= '1';

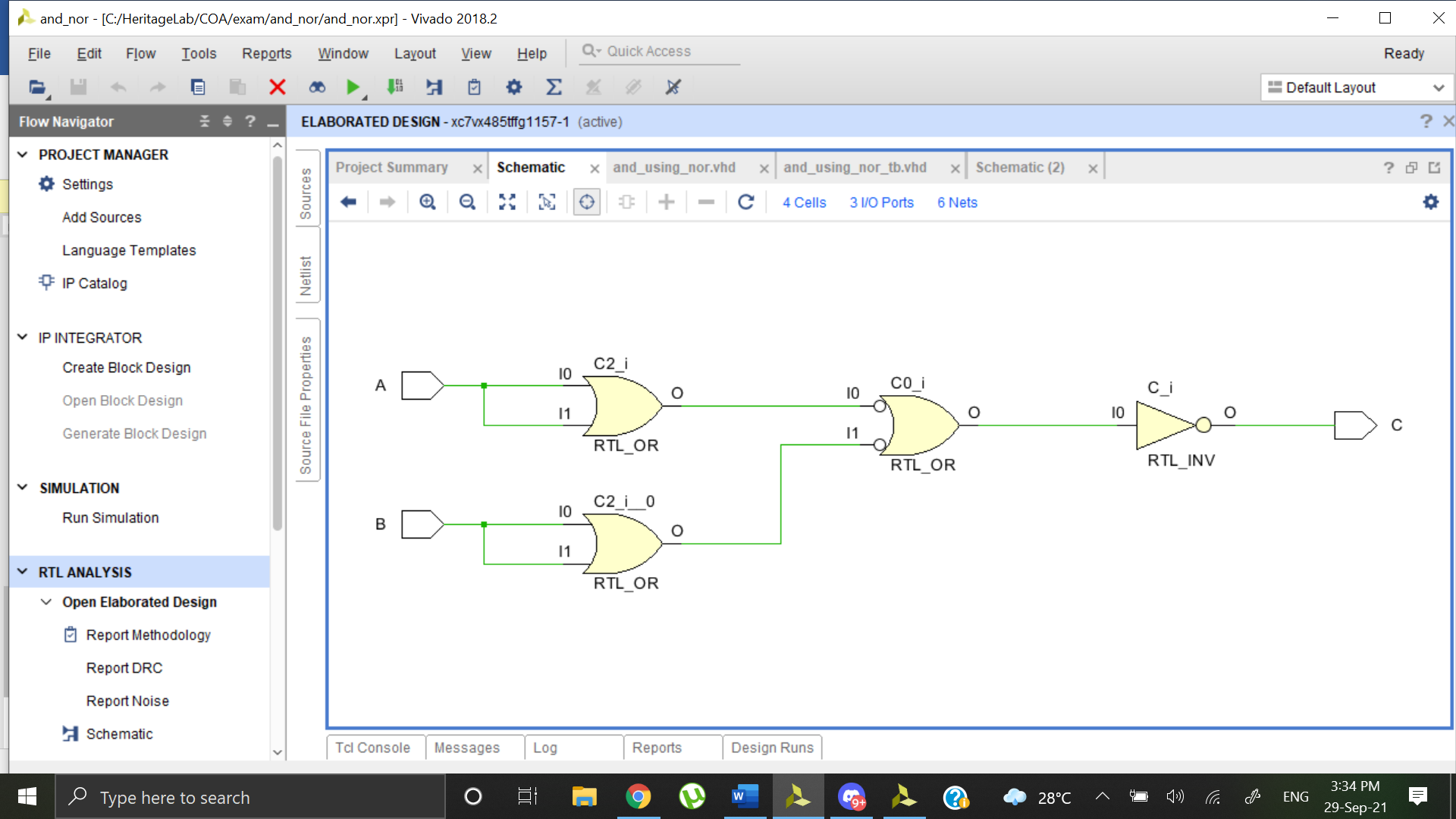
B1<= '1';

wait;

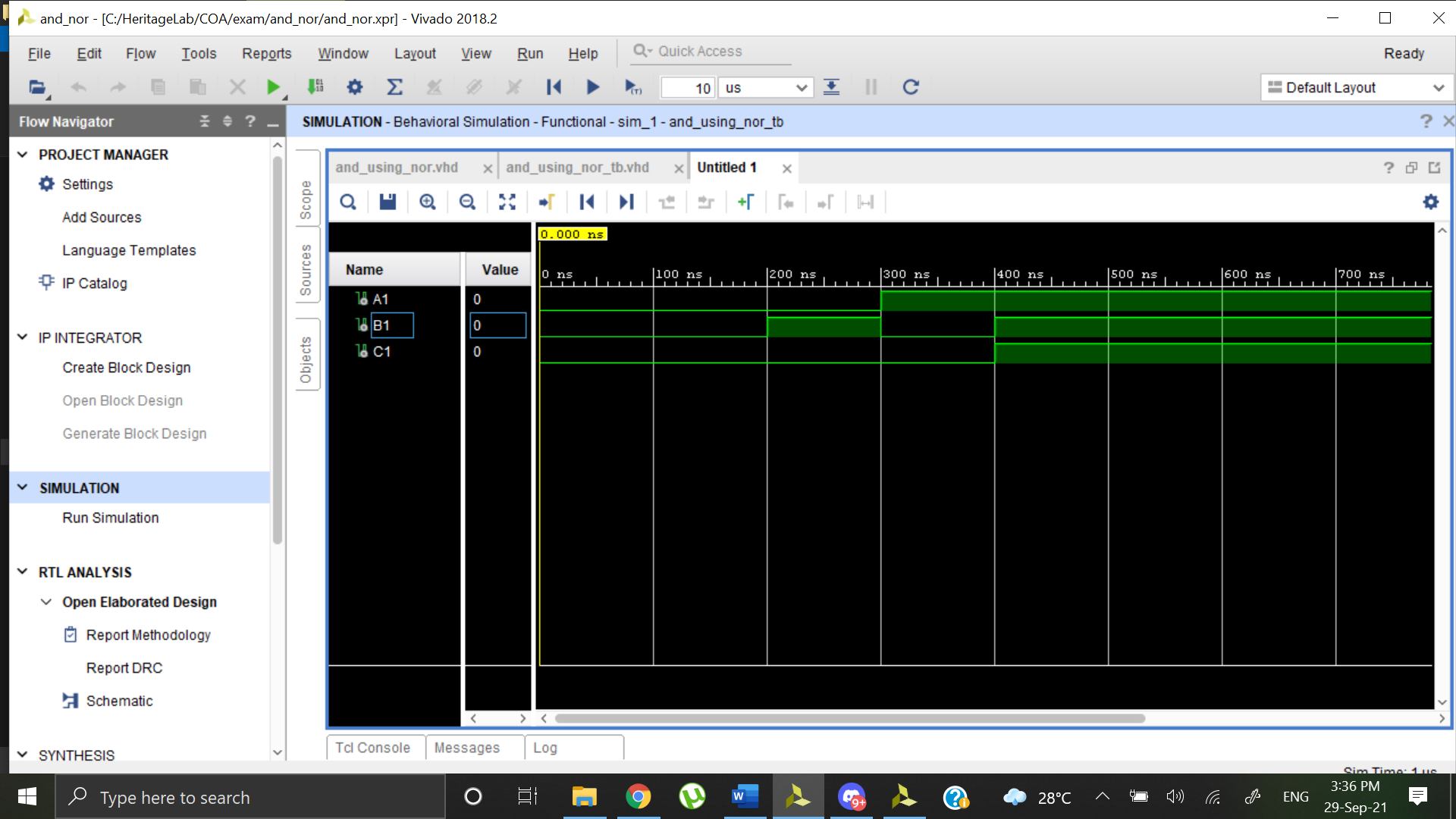
end process;

end Behavioral;

**SCHEMATIC**



**OUTPUT WAVEFORM**



**NOT USING NOR**

**Dataflow Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity not\_using\_nor is

Port ( A : in STD\_LOGIC;

B : out STD\_LOGIC);

end not\_using\_nor;

architecture Behavioral of not\_using\_nor is

begin

B<= A NOR A;

end Behavioral;

**Test Bench Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity not\_using\_nor\_tb is

-- Port ( );

end not\_using\_nor\_tb;

architecture Behavioral of not\_using\_nor\_tb is

component not\_using\_nor is

Port ( A : in STD\_LOGIC;

B : out STD\_LOGIC);

end component;

signal A1 : STD\_LOGIC := '0';

signal B1 : STD\_LOGIC;

begin

uut: not\_using\_nor port map (A=>A1, B=>B1);

stim\_proc: process

begin

wait for 100ns;

A1 <= '0';

wait for 100ns;

A1 <= '0';

wait for 100ns;

A1 <= '1';

wait for 100ns;

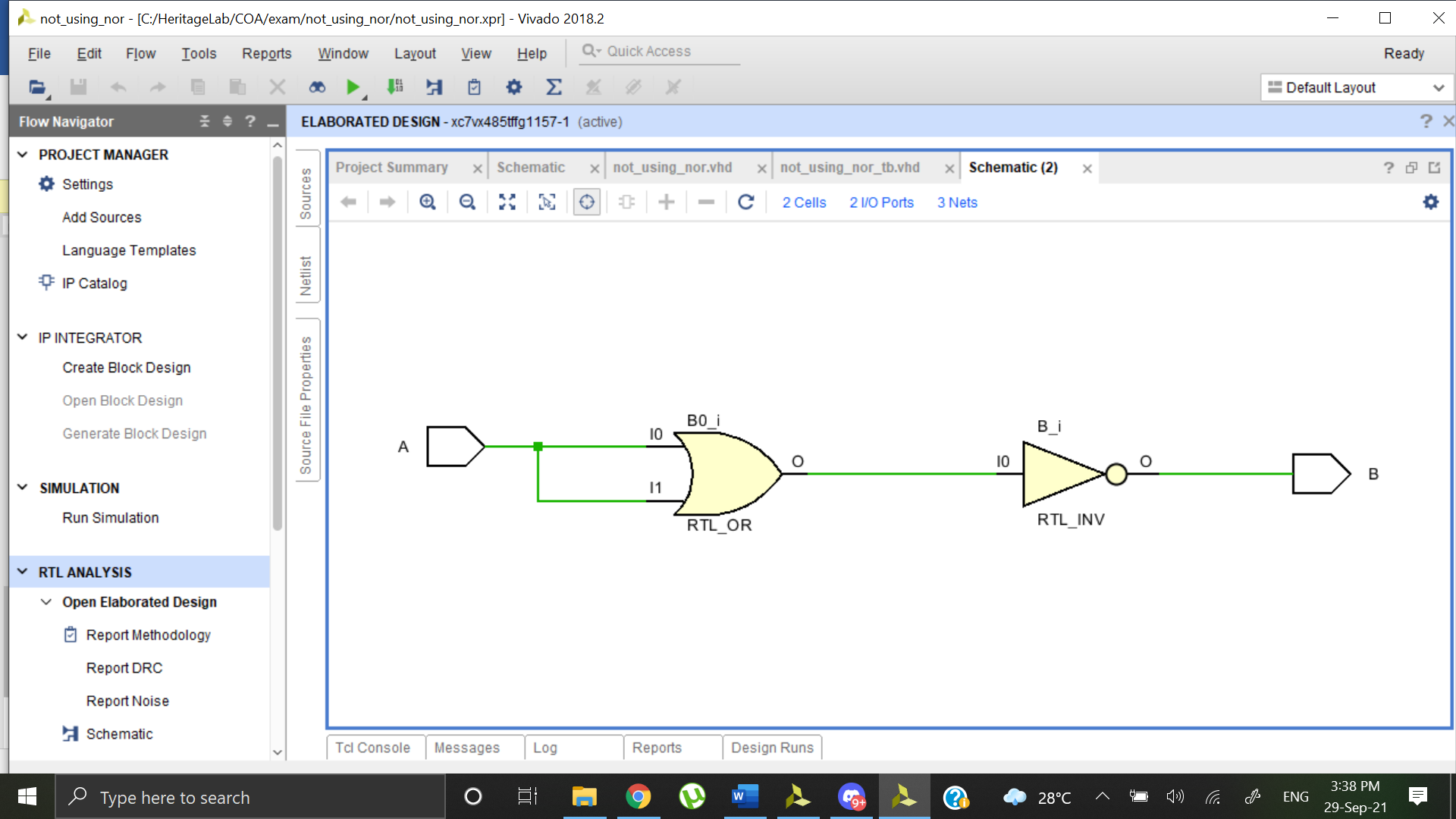
A1 <= '1';

wait;

end process;

end Behavioral;

**SCHEMATIC**



**OUTPUT WAVEFORM**

